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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,323	01/05/2001	Masatoshi Akagawa	1081.1102	3680

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,323	AKAGAWA, MASATOSHI	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14, 16, 17* is/are allowed.

6)☒ Claim(s) *4-6 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

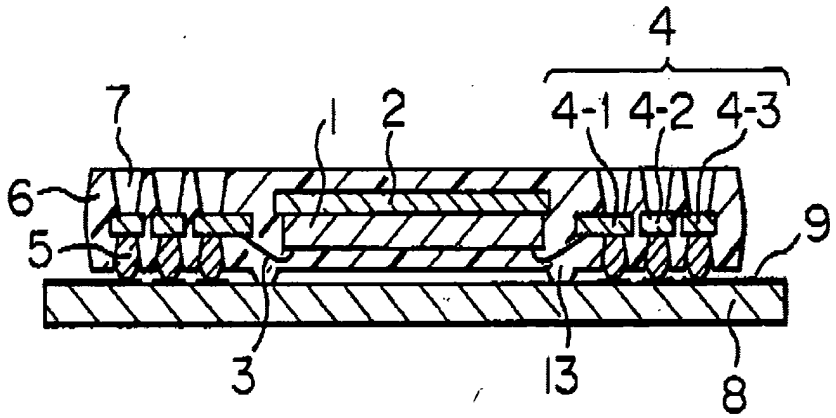
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitano et al. (U.S. Patent 5,608,265).

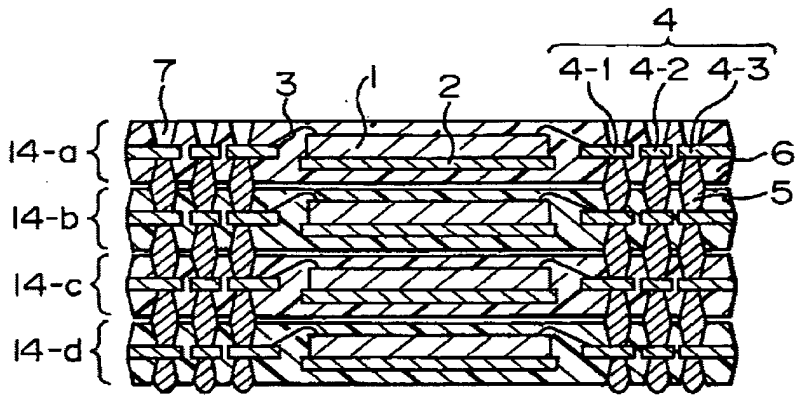
In re claim 18, **Kitano** discloses a semiconductor device multichip package comprising: a substrate having a main surface; a plurality of device layers (**14-a, 14-b, 14-c, 14d**) stacked in succession on the main surface of the substrate wherein each of the plural device layers comprises: a set of conductors comprising a wiring pattern (**3, 4-1, 4-2, 4-3**) (col. 5, line 63 to col. 6, line 10 and FIGS. 9-10); and

FIG. 9



insulating layer **6** formed on and embedding the set of conductors (**3, 4-1, 4-2, 4-3**) and having vias **7** extending therethrough (col. 6, lines 12-23 and FIGS. 9-10), and

FIG. 10



wherein a wiring pattern of a first device layer is electrically connected to a first semiconductor element **1** embedded in a first insulating layer **6** with a first set of conductors (**3, 4-1, 4-2, 4-3**) and one or more of a second set of second set of conductors (located in the upper package 14-c, unlabeled) is/are electrically connected to the first semiconductor element **1** in a second insulating layer (located in the upper package 14-c, unlabeled) and through corresponding the vias **7** to one or more of the first set of conductors (col. 8, lines 10-27 and FIGS. 9-10).

In re claim 19, **Kitano** discloses that: the semiconductor elements **1** are commonly disposed within the respective insulating layers **6** and aligned in the plural, stacked device layers (packages 14-a, 14-b, 14-c, 14-d) (col. 5, line 63 to col. 6, line 23 and FIG. 10).

In re claim 20, **Kitano** discloses that the semiconductor device according to claim 18, further comprising: plural semiconductor elements **1** (one in each individual packages 14-a. 14-b, 14-c, 14-d) in each of the plural device layers and commonly disposed therein so as to be in aligned relationship in the stacked layers (col. 5, line 63 to col. 6, line 23 and FIG. 10).

In re claim 21, **Kitano** discloses that the semiconductor device according to claim 18, wherein each insulating layer **6** surrounds and covers "substantially" all of each outer surface of the semiconductor element **1** embedded therein (FIG. 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano et al. (U.S. Patent 5,608,265) in view of Itabashi et al. (U.S. Patent No. 6,300,244).

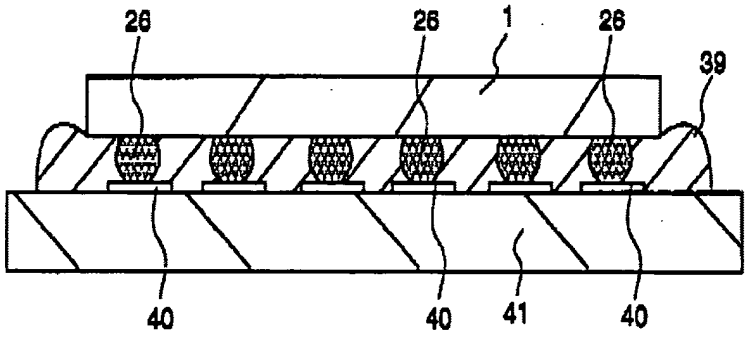
In re claim 4, it is held that the selection of the semiconductor element thickness is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species. In re Jones, 162USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA1980)(discovery of optimum value of result effective variable in a known process is obvious). Note that the specification contains no

disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claims 5-6, **Kitano** does not explicitly disclose that each semiconductor element is electrically connected by flip chip mounting to respective wiring pattern and wherein each semiconductor element is electrically connected via an anisotropically conductive film to respective wiring pattern.

Itabashi, however, discloses in figures 1-11 and related text that each semiconductor element **1** is electrically connected by flip chip mounting to respective wiring pattern, and inherently, by an anisotropically conductive film (figure 10 and col. 17, lines 10-30).

FIG.10



Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Itabashi with the method of

Kitano in order to provide excellent anti-shock resistance and connection reliability (col. 3, lines 35-45, Itabashi).

Allowable Subject Matter

Claim 14, 16 and 17 allowed.

The following is a statement of reasons for the indication of allowable subject matter: (See Applicant's arguments in the Response submitted on July 27th, 2004, on page.2, lines 15-24).

Response to Applicant's Amendment and Arguments

Applicant's arguments filed July 6th, 2005 have been fully considered but they are not persuasive.

Applicant contends that the multichip package of the present claimed invention is not separable into individual packages for each chip, but rather, is a construct of cooperating elements in a single multichip package.

In response to Applicant's contention that the reference, Kitano et al. (U.S. Patent 5,608,265), herein known as Kitano does not explicitly disclose a multichip package. Applicant stated that Kitano recites a plurality of chip packages.

In response to applicant's arguments that Kitano discloses a plurality of chip packages but does not explicitly teach or suggest a multichip package as recited in Applicant's claimed invention, the recitation [multichip package] has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the

preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

For this reason, Examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
September 12th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER